Remarks/Arguments

Reconsideration of the above-identified application in view of the present amendment is respectfully requested. Claims 26-32 are pending. Claims 27 and 28 have been amended to correct typographical errors.

Claims 26-32 stand rejected as anticipated by Hiiragizawa, US 5,561,390. Anticipation requires a single prior art reference that discloses each element of the claim. W.L. Gore & Associates v. Garlock, Inc., 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983), cert. denied 469 U.S. 851 (1984). Additionally, the single prior art reference must disclose each and every element of the claimed invention, arranged as in the claim. Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 U.S.P.Q. 481, 485 (Fed. Cir. 1984). "There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention". Scripps Clinic & Research Foundation v. Genentech Inc., 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). "The identical invention must be shown in as complete detail as is contained in the ... claim". Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Regarding claim 26, the Office Action (page 2, para. 3) states that the phase lock loop circuit of Hiiragizawa, Fig. 1, discloses "a device having at least first and second communications sections suitable for connection to similar devices along different bi-directional communications links". However, Fig. 1 of Hiiragizawa discloses a phase lock loop circuit generating a reference clock signal (XTALCLK) from an oscillating circuit (11) and providing an output to a data processing unit (1)

a clock transition signal having the same polarity back along the first communications link. Col. 10, lines 7-31 of Hiiragizawa discloses a phase comparator having a first node receiving a reference clock signal, a second node receiving a controlled clock signal and arranged to output a first or second level to a third node in response to the received reference clock signal and controlled clock signal having a different phase or the same phase respectively. This statement that two signals are received at first and second nodes and compared and that an output signal is sent to a third node based upon the results of the comparison does not disclose responding to reception of a clock transition signal along a first communications link by transmitting a clock transition signal having the same polarity back along the first communications link, as recited by claim 26.

Hiiragizawa does disclose a phase comparator which will sometimes (depending upon the relative phases of the reference clock signal and controlled clock signal) respond to reception of a clock signal by transmitting a clock signal having the same polarity. However, Hiiragizawa does not disclose that the received and transmitted signals are received and transmitted along the same first communications link, as recited by claim 26.

The Office Action (page 2, para. 3) still further states that Hiiragizawa, Col. 10, lines 7-31, disclose the second communication section being arranged to respond to reception of a clock transition signal along a second communications link by transmitting a clock transition signal having the opposite polarity back along the second communications link. Col. 10, lines 7-31 of Hiiragizawa, as stated above, discloses a phase comparator having a first node receiving a reference clock signal,

a second node receiving a controlled clock signal and arranged to output a first or second level to a third node in response to the received reference clock signal and controlled clock signal having a different phase or the same phase respectively. This statement that two signals are received at first and second nodes and compared and that an output signal is sent to a third node based upon the results of the comparison does not disclose responding to reception of a clock transition signal along a second communications link by transmitting a clock transition signal having the opposite polarity back along the second communications link, as recited by claim 26.

Hiiragizawa does disclose a phase comparator which will sometimes (depending upon the relative phases of the reference clock signal and controlled clock signal) respond to reception of a clock signal by transmitting a clock signal having the opposite polarity. However, Hiiragizawa does not disclose that the received and transmitted signals are received and transmitted along the same second communications link, as recited by claim 26.

The Specification clearly describes the reception and transmission of clock signals in opposite directions along the same communications link allowing two devices connected along a bi-directional communications link to automatically form an oscillating loop providing a synchronized clock signal for the two devices. Any reasonable interconnection of the circuits of Hiiragizawa does not disclose this response.

Regarding claim 27, the Office Action, page 3, para. 4, states that Hiiragizawa, Col. 3, lines 40-55, discloses that the first communication section holds a first clock logic level as an output when the first communication section is not

connected to another device and the second communication section holds a second clock logic level having an opposite polarity to the first clock logic level as an input when the second communications section is not connected to another device. However, Col. 3, lines 40-55 of Hiiragizawa discloses the operation of the circuit of Fig. 9 and specifically describes how the circuit nodes respond to changes in level of the reference clock signal (XTALCLK) when the phase lock loop is in a phase lock condition resulting in input of a lock signal to the set input (S) of flip flop (91). Hiiragizawa does not disclose a response of a circuit to specific states of the clock signal and XTALCLK signal or how the circuit would respond if the circuit was not connected to another device and thereby not receiving input signals, as recited in claim 27.

Regarding claim 28, the Office Action, page 3, para. 4, states that Hiiragizawa, Col. 3, lines 40-55, discloses that the second communications section holds a first clock logic level as an output when the second communications section is not connected to another device and the first communications section holds a second clock logic level having an opposite polarity to the first clock logic level as an output when the first communications section is not connected to another device. However, as stated above, Col. 3, lines 40-55 of Hiiragizawa discloses the operation of the circuit of Fig. 9 and specifically describes how the circuit nodes respond to changes in level of the reference clock signal (XTALCLK) when the phase lock loop is in a phase lock condition resulting in input of a lock signal to the set input (S) of flip flop (91). Hiiragizawa does not disclose a response of a circuit to specific states of the clock signal and XTALCLK signal or how the circuit would respond if the circuit

was not connected to another device and thereby not receiving input signals, as recited in claim 28.

Additionally, a limitation is inherently disclosed by a reference only if it is necessarily present and a person of ordinary skill in the art would recognize its presence. Crown Operations Int'l Ltd.v. Solutia Inc., 289 F.3d 1367, 1377, 62 USPQ.2d 1917, 1922-1923 (Fed. Cir. 2002). Inherency may not be established by probabilities or possibilities. 289 F.3d at 1377, 62 USPQ at 1923. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. Id.

Regarding claim 29, the Office Action, pages 3-4, para. 6, states that Hiiragizawa inherently discloses linked communication sections forming a loop when the first communication section is linked to the second communication section of another device or vice versa through a bi-directional communications link and wherein the device uses an oscillating clock transition signal passing around the loop as a clock signal for communication along the communications link. However, the phase lock loop of Hiiragizawa does not have an oscillating clock transition signal passing around a loop, as recited by claim 29.

In Fig. 1 of Hiiragizawa , components (13, 14, 15, 16 and 17) are arranged in a loop. The component (17) is a frequency divider so that the VCOCLK signal supplied to frequency divider (17) from VCO (16) and the MCCLK signal sent from frequency divider (17) to the PFC (13) have different frequencies. Hiiragizawa, Col. 17, lines 47-61, disclose that the signal VCOIN supplied to the VCO (16) by the LPF (15) is a DC voltage used to control the frequency of the VCO (16). Thus,

Hiiragizawa does not inherently disclose a loop with an oscillating clock transition signal passing around it, as recited by claim 29.

Regarding claim 30, the Office Action, page 4, para. 7, states that Hiiragizawa inherently discloses that, when the first and second communication sections are first linked, the difference between their held input and output clock logic levels causes oscillating clock transition signals to begin passing around the loop. However, as stated above, Hiiragizawa does not inherently disclose an oscillating clock transition signal passing around a loop, as recited by claim 30.

Claim 26, as well as claims 27-30 which depend from claim 26, are in condition for allowance.

Regarding claim 31, the Office Action (page 4, para. 8) states that the phase lock loop circuit of Hiiragizawa, Fig. 1, discloses "an electronic communication network comprising at least first and second devices connected by at least one bi-directional communications link". However, Fig. 1 of Hiiragizawa discloses a phase lock loop circuit generating a reference clock signal (XTALCLK) from an oscillating circuit (11) and providing an output to a data processing unit (1) comprising a controlled clock signal (VCOCLK) along line 18 and a signal indicating a loss of the reference clock signal (XTALFAIL) along line 19.

Accordingly, the phase lock loop circuit of Fig. 1 of Hiiragizawa generates output signals (18, 19) only and does not have any means for receiving or responding to input signals (i.e., Fig. 1 discloses no input signal). Thus, the phase lock loop circuit of Fig. 1 cannot comprise "at least first and second devices connected by at least one bi-directional communications link", as recited in claim 31,

because the phase lock loop circuit does not receive or respond to input signals, but only generates output signals to the data processing unit (1). Thus, connecting two such phase lock loop circuits together though a bi-directional communication link would have no purpose or affect because neither of the circuits would be able to receive or respond to the signals output from the other circuit.

Further, all links disclosed by Hiiragizawa, Figs. 1-11, are uni-directional links (i.e., an arrowhead at one end only). Hiiragizawa does not disclose a bi-directional communication link between two components or nodes, or two circuit components or nodes which are connected by two uni-directional connections, that one of ordinary skill in the art could reasonably interpret to be a bi-directional communication link.

Consequently, Hiiragizawa does not disclose "an electronic communication network comprising at least first and second devices connected by at least one bi-directional communications link ", as recited in claim 31.

The Office Action (page 4, para. 8) further states that Hiiragizawa, Col. 10, lines 7-31, discloses a loop formed by the first device receiving a clock transition signal along the communications link and sending a clock transition signal having the same polarity back along the communications link and the second device receiving a clock transition signal along the communications link and sending a clock transition signal having the opposite polarity back along the communications link. Col. 10, lines 7-31 of Hiiragizawa discloses a phase comparator having a first node receiving a reference clock signal, a second node receiving a controlled clock signal and arranged to output a first or second level to a third node in response to the received reference clock signal and controlled clock signal having a different phase or the

same phase respectively. This statement that two signals are received at first and second nodes and compared and that an output signal is sent to a third node based upon the results of the comparison does not disclose responding to reception of a clock transition signal along a communications link by transmitting a clock transition signal having the same polarity back along the same communications link, as recited by claim 31.

Hiiragizawa does disclose a phase comparator which will sometimes (depending upon the relative phases of the reference clock signal and controlled clock signal) respond to reception of a clock signal by transmitting a clock signal having the same polarity. However, Hiiragizawa does not disclose that the received and transmitted signals are received and transmitted along the same communications link, as recited by claim 31.

The Office Action (page 4, para. 8) still further states that the second node with opposite polarity of Hiiragizawa, Col. 10, lines 7-31 discloses that first and second devices use oscillating clock transition signals traveling around the loop to provide a clock signal to control data transfer along the communications link. Col. 10, lines 7-31 of Hiiragizawa, as stated above, discloses a phase comparator having a first node receiving a reference clock signal, a second node receiving a controlled clock signal and arranged to output a first or second level to a third node in response to the received reference clock signal and controlled clock signal having a different phase or the same phase respectively. This statement that two signals are received at first and second nodes and compared and that an output signal is sent to a third node based upon the results of the comparison does not disclose

oscillating clock transition signals traveling around a loop to provide a clock signal to control data transfer along the same communications link, as recited by claim 31.

Hiiragizawa does disclose a phase comparator which will sometimes (depending upon the relative phases of the reference clock signal and controlled clock signal) respond to reception of clock signal by transmitting a clock signal having the opposite polarity. However, Hiiragizawa does not disclose that the received and transmitted signals are received and transmitted along the same communications link, as recited by claim 31.

Regarding claim 32, the Office Action, page 5, para. 9, states that Hiiragizawa inherently discloses that the clock transition signals traveling around the loop are used as the clock signal. However, as stated above, Hiiragizawa does not inherently disclose a clock transition signal traveling around a loop, as recited by claim 32.

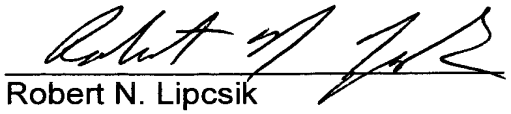
The Specification clearly describes devices connected by bi-directional communication links to automatically and mutually establish a suitable clock signal for data transfer between them. This advantage cannot be achieved by the clock signal generation circuit of Hiiragazawa, which simply generates as an output a clock signal at a predetermined frequency.

Claim 31, as well as claims 32 which depends from claim 31, are in condition for allowance.

In view of the foregoing, it is respectfully requested that the above referenced application is in condition for allowance.

Please charge any deficiency or credit any overpayment in the fees for this amendment to our Deposit Account No. 20-0090.

Respectfully submitted,



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